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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/934,891	08/22/2001	Joseph Weiyeh Ku	10013826-1	8148

7590 04/23/2004

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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/934,891	KU, JOSEPH WEIYEH	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 August 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.4/17/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The attempt to incorporate subject matter into this application by reference to "Analog Method and Circuit for Monitoring Digital Events Performance", by Joseph Weiyeh Ku, docket number 10013825-1 (attorney docket number HPCO.076PA) on page 8, lines 3-4, page 9, lines 11-13 and page 13, lines 17-19 is improper because this reference is now a patent and the docket number information should be replaced with the US patent number 6,600,328 B2, July 29, 2003.

Drawings

2. New corrected drawings are required in this application because the drawings are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1) in view of DeGunther et al. (US 5,519,389).

As per claim 1, Bizjak teaches a circuit arrangement for sampling a logic data signal (figure 8E, page 20, paragraph 310, Bizjak).

However Bizjak does not explicitly teach the specific use of a first timer adapted to time a first time interval; a delay timer coupled to the first timer and adapted to time a delay time interval initiated from the start of the first time interval; a second timer coupled to the delay timer and adapted to time a second time interval initiated at the end of the delay time interval; a coincidence circuit having an input terminal for receiving the logic data signal, an output terminal, and an enable terminal coupled to the second timer, the coincidence circuit adapted to pass a sample of digital event pulses comprising the logic data signal from the input terminal to the output terminal during the second time interval.

DeGunther et al. in an analogous art teach a delay timer having a pulse detector is coupled to sense the input pulses and operate in a pulse sensing standby mode prior to receipt of the first input pulse. The delay timer switches into a time-limited active mode upon receipt of the first input pulse to define a fixed duration delay interval having duration equal to the period of the upper frequency limit of the frequency band. The delay timer switches back into the pulse sensing standby mode upon completion of the delay interval. A gate timer is coupled to an output of the delay timer and switches from a standby mode into a time-limited active mode upon completion of the delay interval to define a fixed duration bandwidth interval. A monitoring circuit includes a first input coupled to the pulse detector to monitor the input pulse train and a second input coupled to monitor an output of the gate timer. The monitoring circuit generates a frequency coincidence signal only if the second input pulse is received during the bandwidth interval to indicate the presence of input pulses having a frequency within the predetermined frequency band (col. 2, lines 31-50, DeGunther et al.)

DeGunther et al. also teach that referring now to FIGS. 2-4, digital frequency discriminator 10 includes a delay timer 16, a gate timer 18 and a coincidence detector a monitoring circuit 20 as illustrated in the FIG. 2 schematic diagram (figures 2-4, col. 3, lines 59-62, DeGunther et al.). Upon detecting input pulse 24, delay timer 16 switches into a time-limited active mode designated in FIG. 4 by reference number 26 to thereby define a fixed duration delay interval having duration T.sub.1 (col. 4, lines 7-10, DeGunther et al.). At the end of delay timer interval T.sub.1 designated by reference number 28, the output of delay timer 16

transitions from a low logic level to a high logic level, switching delay timer 16 back into the pulse sensing standby mode designated in the timing diagrams by reference number 30 (col. 4, lines 13-17, DeGunther et al.). The end of period up going transition of delay timer 16 is designated by reference number 28. That transition is coupled to the input of gate timer 18 and switches the gate timer from a standby mode designated by reference number 36 into a time-limited active mode designated by reference number 38 to define a fixed duration bandwidth interval equal in duration to the period T.sub.2 of gate timer 18 (col. 4, lines 23-29, DeGunther et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of DeGunther et al. by including an additional step of using a first timer adapted to time a first time interval; a delay timer coupled to the first timer and adapted to time a delay time interval initiated from the start of the first time interval; a second timer coupled to the delay timer and adapted to time a second time interval initiated at the end of the delay time interval; a coincidence circuit having an input terminal for receiving the logic data signal, an output terminal, and an enable terminal coupled to the second timer, the coincidence circuit adapted to pass a sample of digital event pulses comprising the logic data signal from the input terminal to the output terminal during the second time interval.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to define a fixed duration time interval during which digital signal can be sampled for analysis.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1) and DeGunther et al. (US 5,519,389) as applied to claim 1 above, and further in view of Stackhouse et al. (US 4,519,090).

As per claim 2, Bizjak and DeGunther et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Bizjak and DeGunther et al. do not explicitly teach the specific use of the circuit arrangement, wherein the first timer is a binary count register having N+1 bits, the delay timer is a latch register having N bits, and the binary count register and latch register are coupled to a comparator circuit, and the

comparator circuit adapted to initiate the second timer when the value of the binary count register and the value of the latch register are equivalent.

Stackhouse et al. in an analogous art teach that the testable time delay includes a flip-flop with a time-delayed latch (col. 1, lines 41-42, Stackhouse et al.). Stackhouse et al. also teach that the data output terminals of the down counter 18, the up counter 34 and the front panel switches 22 are coupled to predetermined positions of the results register 32. These three data states are compared through a self test protocol to assure that the sum of the data outputs of the up counter 34 and the down counter 18 is always equal to the setting of the front panel switches 22 (figures 1A, 1B, col. 2, lines 40-46, Stackhouse et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Stackhouse et al. by including an additional step of using the circuit arrangement, wherein the first timer is a binary count register having N+1 bits, the delay timer is a latch register having N bits, and the binary count register and latch register are coupled to a comparator circuit, and the comparator circuit adapted to initiate the second timer when the value of the binary count register and the value of the latch register are equivalent.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to delay the time interval to start sampling the digital signal for analysis.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389) and Stackhouse et al. (US 4,519,090) as applied to claim 2 above, and further in view of Marsh et al. (US 6,499,656 B1).

As per claim 3, Bizjak, DeGunther et al. and Stackhouse et al. substantially teach the claimed invention described in claim 2 (as rejected above).

However Bizjak, DeGunther et al. and Stackhouse et al. do not explicitly teach the specific use of the circuit arrangement, wherein the delay timer is adapted to pseudo- randomly vary the delay time interval.

Marsh et al. in an analogous art teach the random delay timer consists of a pseudorandom number generator 68 and a counter 70. The counter 70 counts down and when it reaches 0 it generates a trigger

signal 72. The trigger signal 72 causes the pseudo-random generator 68 to calculate a new random number which is then loaded into the counter 70 to time the next random delay period (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Marsh et al. by including an additional step of using the circuit arrangement, wherein the delay timer is adapted to pseudo- randomly vary the delay time interval.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to pseudo- randomly delay the time interval to start sampling the digital signal for analysis and it will provide a large number of different digital signal values for analysis.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Stackhouse et al. (US 4,519,090) and Marsh et al. (US 6,499,656 B1) as applied to claim 3 above, and further in view of Takahashi et al. (US 4,320,962).

As per claim 4, Bizjak, DeGunther et al., Stackhouse et al. and Marsh et al. substantially teach the claimed invention described in claim 3 (as rejected above).

However Bizjak, DeGunther et al., Stackhouse et al. and Marsh et al. do not explicitly teach the specific use of the circuit arrangement, wherein the delay timer is adapted to select the delay time interval from a finite set of discrete times.

Takahashi et al. in an analogous art teach that the timer times setting the delay times in the main and the auxiliary scanning direction for combining the originals (namely, the set times of the preset timers such as T.sub.1, T.sub.2, T.sub.3, t.sub.1, t.sub.2, t.sub.3, etc. in the foregoing example) can be set in accordance with the measurements of the lengthwise and lateral positions on the originals to be combined. The preset timer concerned with the delay times T.sub.1 and T.sub.2 in the auxiliary scanning direction may be a preset counter driven by LSP or RSP, while the preset timer concerned with the delay times t.sub.1, t.sub.2, . . . in the main scanning direction may be a preset counter driven by clock CL (col. 6, lines 13-19, lines 25-30, Takahashi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Takahashi et al. by including an additional step of using the circuit arrangement, wherein the delay timer is adapted to select the delay time interval from a finite set of discrete times.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to delay the time interval using a specific time delay value to start sampling the digital signal for analysis and it will provide a specific number of digital signal values related to the time delay intervals selected.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Stackhouse et al. (US 4,519,090) and Marsh et al. (US 6,499,656 B1) as applied to claim 3 above, and further in view of Sparks (US 6,034,738).

As per claim 5, Bizjak, DeGunther et al., Stackhouse et al. and Marsh et al. substantially teach the claimed invention described in claim 3 (as rejected above).

However Bizjak, DeGunther et al., Stackhouse et al. and Marsh et al. do not explicitly teach the specific use of the circuit arrangement, wherein the latch register is a latching shift register.

Sparks in an analogous art teaches that synchronization of repay image and OSD may be achieved by various methods, for example, by means of a delay using a clocked data latch, shift register (col. 6, lines 62-65, Sparks).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Sparks by including an additional step of using the circuit arrangement, wherein the latch register is a latching shift register.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit arrangement, wherein the latch register is a latching shift register would provide the opportunity to shift and hold the values and provide a random value.

- As per claim 6, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al. and Sparks teach the additional limitations.

Marsh et al. teach the circuit arrangement further comprising a pseudo-random number generator coupled to the latch register, the pseudo-random number generator having less bits than the latch register and the pseudo-random number generator adapted to seed the latch register (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Stackhouse et al. (US 4,519,090), Marsh et al. (US 6,499,656 B1) and Sparks (US 6,034,738) as applied to claim 6 above, and further in view of Clark et al. (US 6,516,384 B1).

As per claim 7, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al. and Sparks substantially teach the claimed invention described in claim 6 (as rejected above).

However Bizjak, DeGunther et al., Stackhouse et al., Marsh et al. and Sparks do not explicitly teach the specific use of the circuit arrangement, wherein the latching shift register is a round robin latch.

Clark et al. in an analogous art teach that round robin register 200 latches are coupled such that after assertion of the round robin reset signal, all latches except latch 210 are cleared (figure 2, col. 3, lines 26-28, Clark et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Clark et al. by including an additional step of using the circuit arrangement, wherein the latching shift register is a round robin latch.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit arrangement, wherein the latching shift register is a round robin latch would provide the opportunity to shift and wrap around the stored values and provide a random value.

- As per claim 8, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks and Clark et al. teach the additional limitations.

DeGunther et al. teach the circuit arrangement wherein the second timer is a second binary counter having M+1 bits, M being less than or equal to N (col. 9, lines 33--37, DeGunther et al.).

11. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Stackhouse et al. (US 4,519,090), Marsh et al. (US 6,499,656 B1), Sparks (US 6,034,738) and Clark et al. (US 6,516,384 B1) as applied to claim 8 above, and further in view of Nakatsu (US 4,339,759).

As per claim 9, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks and Clark et al. substantially teach the claimed invention described in claim 8 (as rejected above).

However Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks and Clark et al. do not explicitly teach the specific use of the circuit arrangement, wherein the first timer is adapted to time a series of periodic first time intervals.

Nakatsu in an analogous art teaches dual timer integrated circuit means comprising a free running timer which fires at selected time intervals (col. 1, lines 66-68, Nakatsu).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Nakatsu by including an additional step of using the circuit arrangement, wherein the first timer is adapted to time a series of periodic first time intervals.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit arrangement, wherein the first timer is adapted to time a series of periodic first time intervals would provide the opportunity to sample the digital data for analysis at regular time intervals.

- As per claim 10, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks, Clark et al. and Nakatsu teach the additional limitations.

Nakatsu teaches the circuit arrangement, wherein the delay timer is adapted to determine and time a new delay time interval for each first time interval in the series of first time intervals (col. 1, lines 66-68, col. 2, lines 1-3, Nakatsu).

12. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Stackhouse et al. (US 4,519,090), Marsh et al. (US 6,499,656 B1), Sparks (US 6,034,738), Clark et al. (US 6,516,384 B1) and Nakatsu (US 4,339,759) as applied to claim 10 above, and further in view of McSorley et al. (US 3,882,492).

As per claim 11, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks, Clark et al. and Nakatsu substantially teach the claimed invention described in claim 10 (as rejected above).

However Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks, Clark et al. and Nakatsu do not explicitly teach the specific use of the circuit arrangement, further comprising a counting circuit coupled to the output terminal of the coincidence circuit, the counting circuit adapted to accumulate a count of the digital event pulses in the sample.

McSorley et al. in an analogous art teach a receiver in which the digital display device includes a counter, and the receiver further includes an oscillator for feeding pulses to the counter in response to a detected change of signal level on one of the inputs to the encoder, a coincidence detector connected to compare the output of the encoder representing the number of the remote station associated with the change of signal level with the number present in the counter, and inhibiting means connected to receive an output from the coincidence detector when the two numbers being compared are equal for inhibiting the supply of pulses to the counter such that the final number displayed by the counter represents the number of the remote station (col. 4, lines 14-27, McSorley et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of McSorley et al. by including an additional step of using the circuit arrangement, further comprising a counting circuit coupled to the output terminal of the coincidence circuit, the counting circuit adapted to accumulate a count of the digital event pulses in the sample.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to count the digital signal pulses for a sample time period and conduct analysis.

- As per claim 12, Bizjak, DeGunther et al., Stackhouse et al., Marsh et al., Sparks, Clark et al., Nakatsu and McSorley et al. teach the additional limitations.

McSorley et al. teach the circuit arrangement, wherein the counting circuit is reset responsive to the first timer (col. 2, lines 64-67, McSorley et al.).

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1) in view of DeGunther et al. (US 5,519,389) and Marsh et al. (US 6,499,656 B1).

As per claim 13, Bizjak teaches a circuit arrangement for sampling a plurality of digital event pulses (figure 8E, page 20, paragraph 310, Bizjak).

However Bizjak does not explicitly teach the specific use of a first timer adapted to time a plurality of base time intervals; a second timer adapted to generate a sampling window signal for a sampling window time interval, the sampling window time interval being a shorter time than any of the base time intervals; a sample window initiate circuit coupled to the first timer; and a sampler circuit coupled to the second timer and arranged to receive the plurality of digital event pulses and to pass a sample of digital event pulses responsive to the sampling window signal.

DeGunther et al. in an analogous art teach a delay timer having a pulse detector is coupled to sense the input pulses and operate in a pulse sensing standby mode prior to receipt of the first input pulse. The delay timer switches into a time-limited active mode upon receipt of the first input pulse to define a fixed duration delay interval having duration equal to the period of the upper frequency limit of the frequency band. The delay timer switches back into the pulse sensing standby mode upon completion of the delay interval. A gate timer is coupled to an output of the delay timer and switches from a standby mode into a time-limited active mode upon completion of the delay interval to define a fixed duration bandwidth interval. A monitoring circuit includes a first input coupled to the pulse detector to monitor the input pulse train and a second input coupled to monitor an output of the gate timer. The monitoring circuit generates a frequency coincidence signal only if the second input pulse is received during the bandwidth interval to indicate the presence of input pulses having a frequency within the predetermined frequency band (col. 2, lines 31-50, DeGunther et al.)

DeGunther et al. also teach that referring now to FIGS. 2-4, digital frequency discriminator 10 includes a delay timer 16, a gate timer 18 and a coincidence detector a monitoring circuit 20 as illustrated in the FIG. 2 schematic diagram (figures 2-4, col. 3, lines 59-62, DeGunther et al.). Upon detecting input pulse 24, delay timer 16 switches into a time-limited active mode designated in FIG. 4 by reference number 26 to thereby define a fixed duration delay interval having duration T.sub.1 (col. 4, lines 7-10, DeGunther et al.).

At the end of delay timer interval T.sub.1 designated by reference number 28, the output of delay timer 16 transitions from a low logic level to a high logic level, switching delay timer 16 back into the pulse sensing standby mode designated in the timing diagrams by reference number 30 (col. 4, lines 13-17, DeGunther et al.). The end of period up going transition of delay timer 16 is designated by reference number 28. That transition is coupled to the input of gate timer 18 and switches the gate timer from a standby mode designated by reference number 36 into a time-limited active mode designated by reference number 38 to define a fixed duration bandwidth interval equal in duration to the period T.sub.2 of gate timer 18 (col. 4, lines 23-29, DeGunther et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of DeGunther et al. by including an additional step of using a first timer adapted to time a plurality of base time intervals; a second timer adapted to generate a sampling window signal for a sampling window time interval, the sampling window time interval being a shorter time than any of the base time intervals; a sample window initiate circuit coupled to the first timer; and a sampler circuit coupled to the second timer and arranged to receive the plurality of digital event pulses and to pass a sample of digital event pulses responsive to the sampling window signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to define a fixed duration time interval during which digital signal can be sampled for analysis.

Bizjak also does not explicitly teach the specific use of starting the second timer at a pseudo-random time within each of the plurality of base time intervals.

Marsh et al. in an analogous art teach the random delay timer consists of a pseudorandom number generator 68 and a counter 70. The counter 70 counts down and when it reaches 0 it generates a trigger signal 72. The trigger signal 72 causes the pseudo-random generator 68 to calculate a new random number which is then loaded into the counter 70 to time the next random delay period (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Marsh et al. by including an additional step of use of starting the second timer at a pseudo-random time within each of the plurality of base time intervals. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to pseudo- randomly delay the time interval to start sampling the digital signal for analysis and it will provide a large number of different digital signal values for analysis.

14. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389) and Marsh et al. (US 6,499,656 B1) as applied to claim 13 above, and further in view of McSorley et al. (US 3,882,492).

As per claim 14, Bizjak, DeGunther et al. and Marsh et al. substantially teach the claimed invention described in claim 13 (as rejected above).

However Bizjak, DeGunther et al. and Marsh et al. do not explicitly teach the specific use of the circuit arrangement, further comprising a counting circuit coupled to the sampler circuit, the counting circuit adapted to accumulate a count of the sample of digital event pulses.

McSorley et al. in an analogous art teach a receiver in which the digital display device includes a counter, and the receiver further includes an oscillator for feeding pulses to the counter in response to a detected change of signal level on one of the inputs to the encoder, a coincidence detector connected to compare the output of the encoder representing the number of the remote station associated with the change of signal level with the number present in the counter, and inhibiting means connected to receive an output from the coincidence detector when the two numbers being compared are equal for inhibiting the supply of pulses to the counter such that the final number displayed by the counter represents the number of the remote station (col. 4, lines 14-27, McSorley et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of McSorley et al. by including an additional step of using the circuit arrangement, further comprising a counting circuit coupled to the sampler circuit, the counting circuit adapted to accumulate a count of the sample of digital event pulses.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to count the digital signal pulses for a sample time period and conduct analysis.

- As per claim 15, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. teach the additional limitations.

McSorley et al. teach the circuit arrangement, wherein the counting circuit is a digital counter (col. 4, lines 14-15, McSorley et al.).

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1) and McSorley et al. (US 3,882,492) as applied to claim 14 above, and further in view of Lai (US 3,801,834).

As per claim 16, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. substantially teach the claimed invention described in claim 14 (as rejected above).

However Bizjak, DeGunther et al., Marsh et al. and McSorley et al. do not explicitly teach the specific use of the circuit arrangement, wherein the counting circuit further comprises a capacitor coupled through a transistor to a constant current source, the transistor being responsive to each of the digital event pulses to pass a substantially fixed amount of charge from the constant current source to the capacitor.

Lai in an analogous art teaches a pulse counter means having an input and output, said input being coupled electrically to the output electrode of said AND gate for counting pulses received therefrom and said output being connectible to digital display means for displaying the number of pulses counted thereby, an analog to pulse width converter circuit, said last-mentioned circuit including in combination: a monostable multivibrator having an input and an output and being operable to a first, stable and second, unstable state, said multivibrator including first and second transistors each having a base, collector and emitter electrode and a capacitor coupled electrically between the collector of said first transistor and the base of said second transistor, said multivibrator input coupled to the junction of said capacitor and the collector of said first transistor, and said multivibrator output being coupled electrically to the collector of said second transistor, constant current source means coupled electrically to the junction of said capacitor and the base electrode of said second transistor, said capacitor being charged in a first

direction to a voltage potential determined by an analog voltage applied to said multivibrator input and trigger circuit means coupled electrically to said multivibrator providing a trigger pulse for operation of said multivibrator from said first, stable to said second, unstable state to produce a resulting voltage potential at the output thereof, said constant current source charging said capacitor in a direction opposite from said first direction upon operation of said multivibrator to said second, unstable state, the charging time of said capacitor in said second direction being determined by the voltage potential of the charge on said capacitor produced by said analog voltage, said circuit output being provided to the second one of said inputs of said AND gate for a time period equal to that required to charge said capacitor by said constant current source, said AND gate providing output pulses to said pulse counter means equal in number to the clock pulses provided by said clock circuit means, so long as said output is produced by said analog to pulse width converter circuit, the number of pulses counted by said pulse counter means corresponding to the voltage potential of said analog voltage applied to the input of said analog to pulse width converter circuit (col. 5, lines 43-49, col. 6, lines 1- 38, Lai).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Lai by including an additional step of using the circuit arrangement, wherein the counting circuit further comprises a capacitor coupled through a transistor to a constant current source, the transistor being responsive to each of the digital event pulses to pass a substantially fixed amount of charge from the constant current source to the capacitor.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to count the digital signal pulses for a sample time period and conduct analysis.

16. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1) and McSorley et al. (US 3,882,492) as applied to claim 15 above, and further in view of Popoff et al. (US 4,202,019).

As per claim 17, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. substantially teach the claimed invention described in claim 15 (as rejected above).

However Bizjak, DeGunther et al., Marsh et al. and McSorley et al. do not explicitly teach the specific use of the circuit arrangement, wherein the first timer is a binary counter having N+1 bits, and the second timer is a binary counter having M+1 bits, M being less than or equal to N.

Popoff et al. in an analogous art teach that designation of the counters in pulse interval timers 68a and 68b as 4-bit binary counters is a specific example of a counter that produces 2.sup.n counts during the interval between successive bits, wherein n is a positive integer, 4 in the specific example (col. 9, lines 16-20, Popoff et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Popoff et al. by including an additional step of using the circuit arrangement, wherein the first timer is a binary counter having N+1 bits, and the second timer is a binary counter having M+1 bits, M being less than or equal to N.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to use the binary counter timers that provides accurate time values and one timer can provide longer time interval than the other timer.

- As per claim 18, Bizjak, DeGunther et al., Marsh et al., McSorley et al. and Popoff et al. teach the additional limitations.

Popoff et al. teach the circuit arrangement, wherein the first and second timers are adapted to count clock cycles (col. 9, lines 16-20, Popoff et al.).

Marsh et al. teach the pseudo-random time being a discrete binary value of first timer (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

- As per claim 19, Bizjak, DeGunther et al., Marsh et al., McSorley et al. and Popoff et al. teach the additional limitations.

Marsh et al. teach the circuit arrangement, wherein the sampling window initiate circuit comprises a pseudo-random number generator having K bits coupled to a shift register having N bits, the shift register arranged to receive and shift binary pseudo-random numbers from the pseudo-random number generator

to form N bit pseudo-random numbers, whereby K is less than or equal to N (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

17. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1), McSorley et al. (US 3,882,492) and Popoff et al. (US 4,202,019) as applied to claim 19 above, and further in view of Clark et al. (US 6,516,384 B1).

As per claim 20, Bizjak, DeGunther et al., Marsh et al., McSorley et al. and Popoff et al. substantially teach the claimed invention described in claim 19 (as rejected above).

However Bizjak, DeGunther et al., Marsh et al., McSorley et al. and Popoff et al. do not explicitly teach the specific use of the circuit arrangement, wherein the shift register is a round robin latch.

Clark et al. in an analogous art teach that round robin register 200 latches are coupled such that after assertion of the round robin reset signal, all latches except latch 210 are cleared (figure 2, col. 3, lines 26-28, Clark et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Clark et al. by including an additional step of using the circuit arrangement, wherein the shift register is a round robin latch.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit arrangement, wherein the shift register is a round robin latch would provide the opportunity to shift and wrap around the stored values and provide a random value.

18. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1), McSorley et al. (US 3,882,492), Popoff et al. (US 4,202,019) and Clark et al. (US 6,516,384 B1) as applied to claim 20 above, and further in view of Whitlock et al. (US 4,531,102).

As per claim 21, Bizjak, DeGunther et al., Marsh et al., McSorley et al., Popoff et al. and Clark et al. substantially teach the claimed invention described in claim 20 (as rejected above).

However Bizjak, DeGunther et al., Marsh et al., McSorley et al., Popoff et al. and Clark et al. do not explicitly teach the specific use of the circuit arrangement, wherein the overflow bit of the first timer is coupled to the counting circuit, the counting circuit adapted to reset responsive to the overflow bit of the first timer.

Whitlock et al. in an analogous art teach that the counter 114 is connected to proceed through a six count cycle between conditions corresponding to the counts from 10 to 15 with the overflow pulse at the CY output being used to reset the counter to a count of 10 (figure 2C, col. 10, lines 64-68, Whitlock et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Whitlock et al. by including an additional step of using the circuit arrangement, wherein the overflow bit of the first timer is coupled to the counting circuit, the counting circuit adapted to reset responsive to the overflow bit of the first timer.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the circuit arrangement, wherein the overflow bit of the first timer is coupled to the counting circuit, the counting circuit adapted to reset responsive to the overflow bit of the first timer would provide the opportunity to start counting at the beginning of the time interval of the first timer.

19. Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1) in view of DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1) and McSorley et al. (US 3,882,492).

As per claim 22, Bizjak teaches a method for sampling a logic data signal (figure 8E, page 20, paragraph 310, Bizjak).

However Bizjak does not explicitly teach the specific use of receiving a plurality of digital event pulses characterizing the logic data signal during each of a series of base time intervals and selecting a subset of digital event pulses during application of the sampling window signal.

DeGunther et al. in an analogous art teach a delay timer having a pulse detector is coupled to sense the input pulses and operate in a pulse sensing standby mode prior to receipt of the first input pulse. The delay timer switches into a time-limited active mode upon receipt of the first input pulse to define a fixed

duration delay interval having duration equal to the period of the upper frequency limit of the frequency band. The delay timer switches back into the pulse sensing standby mode upon completion of the delay interval. A gate timer is coupled to an output of the delay timer and switches from a standby mode into a time-limited active mode upon completion of the delay interval to define a fixed duration bandwidth interval. A monitoring circuit includes a first input coupled to the pulse detector to monitor the input pulse train and a second input coupled to monitor an output of the gate timer. The monitoring circuit generates a frequency coincidence signal only if the second input pulse is received during the bandwidth interval to indicate the presence of input pulses having a frequency within the predetermined frequency band (col. 2, lines 31-50, DeGunther et al.)

DeGunther et al. also teach that referring now to FIGS. 2-4, digital frequency discriminator 10 includes a delay timer 16, a gate timer 18 and a coincidence detector a monitoring circuit 20 as illustrated in the FIG. 2 schematic diagram (figures 2-4, col. 3, lines 59-62, DeGunther et al.). Upon detecting input pulse 24, delay timer 16 switches into a time-limited active mode designated in FIG. 4 by reference number 26 to thereby define a fixed duration delay interval having duration T.sub.1 (col. 4, lines 7-10, DeGunther et al.). At the end of delay timer interval T.sub.1 designated by reference number 28, the output of delay timer 16 transitions from a low logic level to a high logic level, switching delay timer 16 back into the pulse sensing standby mode designated in the timing diagrams by reference number 30 (col. 4, lines 13-17, DeGunther et al.). The end of period up going transition of delay timer 16 is designated by reference number 28. That transition is coupled to the input of gate timer 18 and switches the gate timer from a standby mode designated by reference number 36 into a time-limited active mode designated by reference number 38 to define a fixed duration bandwidth interval equal in duration to the period T.sub.2 of gate timer 18 (col. 4, lines 23-29, DeGunther et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of DeGunther et al. by including an additional step of receiving a plurality of digital event pulses characterizing the logic data signal during each of a series of base time intervals and selecting a subset of digital event pulses during application of the sampling window signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to define a fixed duration time interval during which digital signal can be sampled for analysis.

Bizjak also does not explicitly teach the specific use of applying a sampling window signal for a sample window time interval beginning at a pseudo-random time during each of a series of base time intervals.

However Marsh et al. in an analogous art teach the random delay timer consists of a pseudorandom number generator 68 and a counter 70. The counter 70 counts down and when it reaches 0 it generates a trigger signal 72. The trigger signal 72 causes the pseudo-random generator 68 to calculate a new random number which is then loaded into the counter 70 to time the next random delay period (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Marsh et al. by including an additional step of applying a sampling window signal for a sample window time interval beginning at a pseudo-random time during each of a series of base time intervals.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to pseudo- randomly delay the time interval to start sampling the digital signal for analysis and it will provide a large number of different digital signal values for analysis.

Bizjak also does not explicitly teach the specific use of accumulating a count of the subset digital event pulses.

However McSorley et al. in an analogous art teach a receiver in which the digital display device includes a counter, and the receiver further includes an oscillator for feeding pulses to the counter in response to a detected change of signal level on one of the inputs to the encoder (col. 4, lines 14-18, McSorley et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of McSorley et al. by including an additional step of accumulating a count of the subset digital event pulses.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to count the digital signal pulses for a sample time period and conduct analysis.

- As per claim 26, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. teach the additional limitations. Claim 26 follows the same limitations as claim 22. See rejection to claim 22, above. Claim 26 is rejected under the same rational as to claim 22 rejected above.

20. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1) and McSorley et al. (US 3,882,492) as applied to claim 22 above, and further in view of Popoff et al. (US 4,202,019).

As per claim 23, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. substantially teach the claimed invention described in claim 22 (as rejected above).

However Bizjak, DeGunther et al., Marsh et al. and McSorley et al. do not explicitly teach the specific use of the method, further comprising: timing each base time interval with a base time binary counter, the base time binary counter adapted to count clock cycles; and timing the sample window time interval with a sample window binary counter, the sample window binary counter adapted to count clock cycles.

Popoff et al. in an analogous art teach that designation of the counters in pulse interval timers 68a and 68b as 4-bit binary counters is a specific example of a counter that produces 2.sup.n counts during the interval between successive bits, wherein n is a positive integer, 4 in the specific example (col. 9, lines 16-20, Popoff et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Popoff et al. by including an additional step of using the method, further comprising: timing each base time interval with a base time binary counter, the base time binary counter adapted to count clock cycles; and timing the sample window time interval with a sample window binary counter, the sample window binary counter adapted to count clock cycles.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to use the binary counter timers that provides accurate time values and one timer can provide longer time interval than the other timer.

21. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizjak (US 2002/0103619 A1), DeGunther et al. (US 5,519,389), Marsh et al. (US 6,499,656 B1) and McSorley et al. (US 3,882,492) and Popoff et al. (US 4,202,019) as applied to claim 23 above, and further in view of Clark et al. (US 6,516,384 B1).

As per claim 24, Bizjak, DeGunther et al., Marsh et al. and McSorley et al. and Popoff et al. substantially teach the claimed invention described in claim 23 (as rejected above).

Marsh et al. also teach the method, further comprising: seeding a round robin latch with a pseudo-random number generator, the latch having a length of N bits, the base time counter having a length of N+1 bits, and the pseudo-random number generator having fewer bits than the round robin latch; shifting latch bit values and populating all bits of the latch; forming an N bit pseudo-random number in the latch; and initiating timing of the sample window time interval when a value of the base time binary counter is equivalent to a value of the latch (figure 3, col. 8, lines 46-48, lines 52-57, Marsh et al.).

However Bizjak, DeGunther et al., Marsh et al. and McSorley et al. and Popoff et al. do not explicitly teach the specific use of a round robin latch.

Clark et al. in an analogous art teach that round robin register 200 latches are coupled such that after assertion of the round robin reset signal, all latches except latch 210 are cleared (figure 2, col. 3, lines 26-28, Clark et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bizjak's patent with the teachings of Clark et al. by including an additional step of using a round robin latch.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a round robin latch would provide the opportunity to shift and wrap around the stored values and provide a random value.

- As per claim 25, Bizjak, DeGunther et al., Marsh et al. and McSorley et al., Popoff et al. and Clark et al. teach the additional limitations.

McSorley et al. teach the method, further comprising resetting the count of the subset of digital event pulses accumulated at the end of each base time interval (col. 2, lines 64-67, McSorley et al.).

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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